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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,325	01/05/2001	Tomohiro Yamashita	201540US2	3684

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ALEXANDRIA, VA 22314

EXAMINER
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NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/754,325

Applicant(s)

YAMASHITA ET AL.

Examiner

ori nadav

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MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 August 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 11-14 is/are rejected.
- 7) ☒ Claim(s) 10 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support for the claimed limitations of a first conductive layer formed from one side of the first and second wells to their other side (i.e. a first conductive layer formed across the first well and the second well), as recited in claims 1, 5 and 13.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of a first conductive layer formed from one side of the first and second wells to their other side (i.e. a first conductive layer formed across

the first well and the second well) with an end provided on the first well and another end provided on the second well, as recited in claims 1, 5 and 13, is unclear as to how a first conductive layer can be formed across the first well and the second well (i.e., not terminating in the first and second wells), and at the same time has an end provided on the first well and another end provided on the second well.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, 8-9 and 11, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (6,329,694) in view of Wei et al. (5,843,813).

Regarding claim 1, Lee et al. teach in figure 20 and related text a semiconductor device comprising: semiconductor substrate 90; a first well 101 of a prescribed conductivity type at which a first active transistor element 104 is provided, selectively formed in a surface of the semiconductor substrate; a second well 91 of the same conductivity type as the prescribed conductivity type at which a second active transistor element 94 is provided, selectively formed in the surface

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of the semiconductor substrate; a first conductive layer 106 across the first well and the second well in the surface of the semiconductor substrate with an end provided on the first well and another end provided on the edge of the second well electrically connecting the first well and the second well, and first and second contacts are situated directly above the first and second wells, respectively, wherein the first and second contacts are connected to a single potential  $V_{cc}$ .

Lee et al. do not explicitly state that the first conductive layer has an end provided on the second well.

Wei et al. teach in figure 10B a first conductive layer 246 having an end provided on a first well 264 and another end provided on a second well 274.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the first conductive layer of Lee et al. on the second well in order to simplify the processing steps of making the device.

Regarding claims 2-4, Lee et al. teach in figure 20 a first contact and a second contact being in electrical contact with the first conductive layer, wherein the first contact is arranged in opposition to the first well through the first conductive layer while the second contact is arranged in opposition to the second well through the first conductive layer.

Regarding claim 5, Lee et al. teach in figure 20 and related text a second conductive layer 105 formed in the surface of the semiconductor substrate and

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provided on the first well without being in contact with the second well, wherein the first contact Vcc is in direct contact with the second conductive layer.

Regarding claim 8, Lee et al. teach in figure 20 a second conductive layer includes an impurity introduction layer N+ of the same conductivity type as the prescribed conductivity type N

Regarding claim 9, Lee et al. teach in figure 20 a second conductive layer has lower resistivity (P+) than the first well (N).

Claim 12, insofar as in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. and Wei et al., as applied to claim 5 above, and further in view of Nishigohri (6,384,455).

Lee et al. and Wei et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a second well being deeper than the first well. Nishigohri teaches in figure 16 a second well 31 being deeper than the first well 41. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the second well deeper than the first well in Lee et al.'s device in order to adjust the voltage characteristics of the device.

Claims 6-7, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. and Wei et al., as applied to claim 5 above, and further in view of Suzuki (6,066,520).

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Regarding claim 6, Lee et al. and Wei et al. teach substantially the entire claimed structure, as applied to claim 5 above, except a first conductive layer includes at least one of an impurity introduction layer of the same conductivity type as the prescribed conductivity type and a compound layer of the material for the semiconductor substrate and a metal.

Suzuki teaches in figure 1H a conductive layer 125 including a compound layer of the material for the substrate and a metal formed over a conductive layer 123. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a conductive layer including a compound layer of the material for the substrate and a metal in Lee et al. and Wei et al.'s device in order to reduce the contact resistance of the conductive layer. Note that it is well known in the art to use silicide layer as means to reduce contact resistance.

Regarding claim 7, Lee et al. teach in figure 20 a first conductive layer has lower resistivity (P+) than the first well (N) and the second well (N).

Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuda et al. (5,519,243) in view of Suzuki (6,066,520).

Kikuda et al. teach in figure 3 and related text (column 10, line 20 to column 11, line 12) a semiconductor device comprising: semiconductor substrate 2; a first well 4 of a prescribed conductivity type at which a first active element 14 is provided formed in a surface of the semiconductor substrate; a second well 33 of the same conductivity type as the prescribed conductivity type at which a second

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active element 24 is provided, formed in the surface of the semiconductor substrate; a first conductive layer 6 (a well is a conductive layer) across the first well and the second well in the surface of the semiconductor substrate with an end provided on the first well 4 and another end provided on the second well 33; and first and second contacts Vss directly connected the conductive layer 6 and connected to a single potential Vss.

Kikuda et al. do not teach a conductive layer including a compound layer of the material for the substrate and a metal.

Suzuki teaches in figure 1H a conductive layer 125 including a compound layer of the material for the substrate and a metal formed over a conductive layer 123. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a conductive layer including a compound layer of the material for the substrate and a metal in Kikuda et al.'s device in order to reduce the contact resistance between the first well and the second well. Note that it is well known in the art to use silicide layer as means to reduce contact resistance.

Regarding claim 14, Kikuda et al. teach a conductive layer 6 includes an impurity introduction layer N+ of the same conductivity type as the prescribed conductivity type.

***Allowable Subject Matter***

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Reasons for allowance***

The following is an examiner's statement of reasons for allowance  
Lee et al. and Wei et al. appear to be the closest prior art reference. Lee et al. and Wei et al. teach substantially the entire claimed structure as recited in claims 1-3, except a first well and the second well having different impurity profiles. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

***Response to Arguments***

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the**

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**Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



O.N.  
October 30, 2003

ORI NADAV  
PATENT EXAMINER  
TECHNOLOGY CENTER 2800